Inductively coupled plasma etching for delineation of InAs/GaSb pixels

Jean Nguyen, John Gill, Sir B. Rafol, Alexander Soibel, Arezou Khoskhlagh, David Ting, Sam Keo, Anita Fisher, Edward Luong, John Liu, Jason Mumolo, and Sarath D. Gunapala

Jet Propulsion Laboratory, California Institute of Technology, 4800 Oak Grove Dr. Pasadena, CA, 91109 USA

Abstract

We developed 320x256 Complimentary Barrier Infrared (CBIRD) focal plane array (FPA) for long wave infrared (LWIR) imaging application. The FPA layers grown by molecular beam epitaxy (MBE) had 300 periods 1.9 μm thick absorber. The CBIRD arrays showed the mean dark current density of 2.2 x 10^{-4} A/cm^2, when 128 mV bias voltage was applied. The long wave cut off was observed at 8.8 μm at the 50 % peak and the maximum quantum efficiency was 54 % at 5.6 μm. The arrays had 81 % fill factor with 97 % operability with noise equivalent difference temperature (NEΔT) of 18.6 mK and a mean detectivity of D*=1.3 x 10^{11} Hz$^{1/2}$/W.

Key word: inductively coupled (ICP) plasma dry etching, superlattice detectors, long wavelength infrared, focal plane array, InAs/GaSb

1. Introduction

The need for dry etching process of FPA has been well proven to play an essential role in improving the device performance with high fill-factor, small pitch. The potential impact of the dry etch process on the detector performance justifies the need for complete understanding. The importance of the etch parameters on achieving clean sidewalls, smooth surface morphology, and anisotropic etching has been reported previously [1-3]. However, little to no discussion has been provided on additional factors that play an equally important role on the sidewall quality and device performance.

This article will discuss those additional factors and their effects on the dry etch process for achieving low dark current LWIR CBIRD FPAs. First of all, the dielectric hard mask will be

discussed. Detailed on how to achieve a high density robust mask with excellent pattern transfer will be provided. Then different methods of wafer mounting on the carrier plate will be discussed, which is required to achieve good thermal contact during the etching and maintain a uniform temperature across the wafer. We also compare the results of pixel delineation, using ICP dry etch system, on sparsely populated mesas for test detectors and densely packed pixels for FPAs. The etching process is then demonstrated on a 320x256 CBIRD FPA imaging at 80 K with 8.8 μm cut-off.

2. Growth, fabrication, and characterization

The device structure used in this work is a long-wavelength CBIRD design consisting of an InAs/GaSb superlattice (SL) absorber surrounded by an InAs/GaSb hole barrier and an InAs/GaSb electron barrier [4]. The device is grown on a 50 nm Te doped (100) GaSb substrate in a Veeco Applied-Epi Gen III molecular beam epitaxy chamber. The material is characterized using X ray diffraction (XRD), surface scan, atomic force microscope (AFM), and low temperature photoluminescence (PL). The pixels of the FPA are then fully reticulated down to the bottom contact using an ICP dry etch system. Further detailed information on the etching process will be provided later in this article. Following this, Ti/Pt/Au/Ni/Au ohmic contacts are evaporated on the defined mesa and then indium bumps were deposited on the ohmic contacts. Arrays are individually diced and bonded read-out-integrated-circuit (ROIC) using FC-300 flip chip bonder. Epoxy underfill is applied and then substrate is removed by lapping, followed by another ICP dry etch. The devices are wire bonded and cooled down to 80 K for testing. No AR coating is applied.

3. Dry etch process

Dry etching techniques have been reported in many publications, but external effects which indirectly affects the outcome of pixel delineation has not been properly addressed yet. This includes chamber conditioning and cleanliness, hard mask quality, wafer mounting technique, mask layout, and the wafer size. Each of these will be discussed separately below.

3.1 chamber conditioning and cleanliness.

The cleanliness and the conditioning of the chamber are very important, as it can bring unwanted effects such as re-deposition of particles from the chamber walls. Typically DC bias value is a good indication whether the chamber needs to be cleaned or not. We clean the chamber by SF_6/O_2 plasma cleaning first and then chamber is opened up and wiped out with solvent. Both plasma cleaning and manual wiping out the chamber will remove gas residues and

polymers. Then chamber is pumped down overnight at elevated temperature to drive out moisture. Chamber conditioning is done using the same exact recipe as the SL etch with the silicon carrier wafer in the chamber system and a large GaSb substrate placed on top. Figure 1 plots the dark current density, SL etch rate, and DC bias as a function of the number of hours the system has been conditioned. As can be noted, the bias continues to droop as the system becomes conditioned closer to tis prime state. Once the system reached its prime state, bias, etch rate, and dark current density all begin to stabilize and reach ideal values. due to limitations that the authors experienced with their individual system, the same etch process was used for chamber conditioning as was used for device fabrication, and this lead to slow etch rates and consequently long condition times. The plot shown represents CH_4/H_2 conditioning, but based on our experience, BCl_3/Cl_2 process requires shorter conditioning.

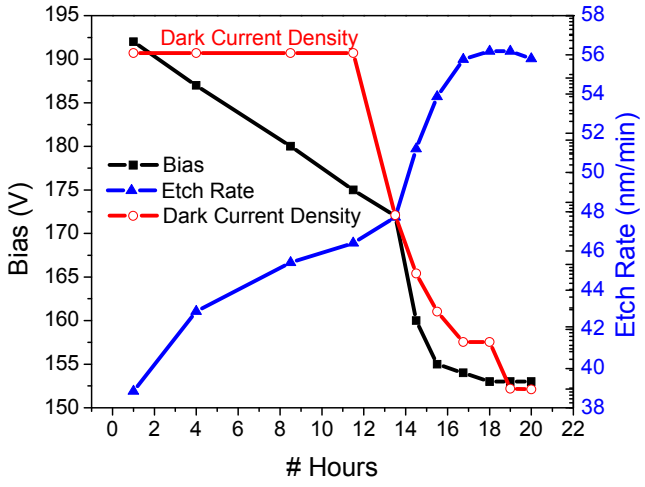

Figure 1. DC Bias, CBIRD dark current density, and SL etch rate for CH_4/H_2 conditioning of the ICP system used at JPL. Shorter conditioning times are expected for BCl_3/Cl_2 plasma.

3.2 dielectric hard mask

For dry etching in the ICP system, a dielectric hard mask was required due to the heating effect the high density plasma has on the photoresist. It is desired for the hard mask to undergo minimal erosion to prevent from interacting with ions or byproducts during the etch process. Furthermore, achieving near-vertical sidewalls with straight edges can only be achieved with the proper pattern transfer. A poor mask with tapered sidewall profile and unwanted ripples will limit the quality of the etched pixels. In order to achieve high quality mask, three categories

were investigated and optimized individually: choice of mask material, material deposition technique, and RIE gases used for mask patterning.

For the dielectric hard mask, there two different materials to choose from: SiO_2 and SiN_x. The choice was made based on the gases used during the ICP etch of the pixels, and the CBIRD structure etch recipe is primarily methane based [1]. For the methane based etching of II-V materials, the formation of polymer during het etch has been reported [5-6]. However, this effect also has been found to be beneficial due to its ability to protect the sidewall from plasma-induced damage [7-8]. Given the potential for O_2 to remove polymers and large amount of unwanted mask erosion and relatively low selectivity that have been observed with SiO_2 in methane/hydrogen based plasma [9], SiN_x was chosen.

For the deposition technique, two different systems were compared: PECVD and ICP PECVD. The ICP PECVD uses ICP as the source, allowing denser higher quality films at lower deposition temperature [10]. The differences between the systems were found to be obvious in both erosion or loss rates during eh etch and also with the sharpness of the mask during pattern definition. For both SiO_2 and SiN_x, less mask waviness and sharper corners were achieved when the films were deposited by ICP-PECVD. Due to the potential degradation whn exposing SL devices to high temperatures, the depositions were performed at a temperature of 150 ^{o} C, and both techniques were independently optimized to achieve the highest mask density. The ICP-PECVD SiN_x appeared to have undergone less erosion during the etching of the SL pixels at a rate of 1.1 nm/min, which was 2.8 times lower than SiN_x deposited by PECVD. To optimize the ICP-PECVD depiction, a higher density was achieved with lower ICP powers and also a gs flow ratio reduced to SiH_4:Ar=3:4, leading to a lower measured refractive index.

To pattern the dielectric hard mask, a simple RIE system was used and two different gas mixtures were compared. Any taper in the hard mask can subsequently limit the sidewwall angle of the FPA pixels, and it was fond that the gas selection played a large role in affecting this taper. Cross-sectional SEM of the same SiN_x mask etched with CF_4/O_2 and CHF_3/Ar are shown in figure 2. For purposes of discerning the large impact, a thick 800 nm mask was deposited. A significant improvement was observed when pattering the hard mask using CHF_3/Ar, achieving a near vertical profile with an angle of 83.2 ^{o}. This is compared to 35.6 ^{o}, achieved with CF_4/O_2 was used. To achieve this near vertical profile in the CHF_3/Ar etch, the gas flow ratio was found to have the largest impact, with an optimal ratio being CHF_3:Ar=2:3. The result of this led to a SL sidewall improvement by at least 8 ^{o}.

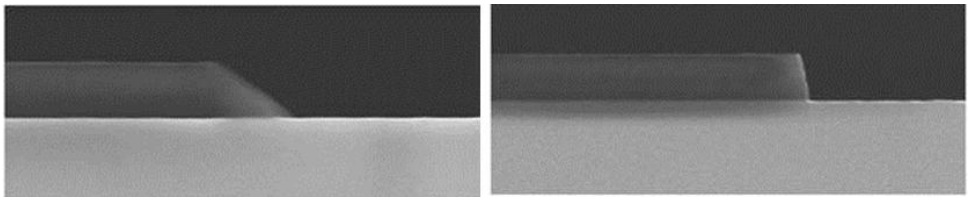

Figure 2. Cross-sectional SEM images of a 800 nm ICP-PECVD deposited SiN_x patterned using (left) CF_4/O_2 and (right) CHF_3/Ar.

3.3 wafer mounting technique.

For good etch uniformity and proper hear transfer, it is important that the proper wafer mounting technique is used. A good mounting technique will use a medium that can be uniformly applied, does not outgas or cause contamination in the chamber, and can be easily removed. In this work, three different media were experimented with: Apezion M high-vacuum grease, fomblin oil, and PR 220-3 photoresist. The high vacuum grease had good thermal contact, but uniform spreading of the grease was hard to achieve and was user dependent, leading to inconsistent results. Formalin oil was very runny and messy to remove. Furthermore, the oil caused issues when the sample was pumped down in the loadlock. The oil would spread out to the edge of the wafer and then on top of the sample, and any material that had been touched by the oil was then damaged. Finally, the photoresist was found to be the best choice amongst the three. The photoresist was spun onto the carrier wafer with a thickness that depended on the size of the wafer and removal post-etch was done using acetone.

3.4 pixel spacing and exposed Epi-grown material

during the developmental stage, quick feedback and reduced optimization times are desired, and this can be done by using test detectors that are made large enough such that the detector scan easily be wire-bonded and the dicing, hybridization, underfill, backside thinning process can be avoided, however, differences in both electrical performance and mechanical characteristics were observed when the same etch process was used for the test detectors and the FPA pixels. Therefore, the optimal parameters for the test detectors will differ from the optimal parameters for the FPA pixels, so an adjustment is required. This was fond to be especially true for chlorine based etches where high volatilities may require a larger amount of adjustment. The reason for this because the FPA pixels are more closely spaced and also there

is a lesser amount of exposed epi-grown material. For this work, the large test detectors are spaced at least 100 μm apart and contain 81.7 % of exposed epi-grown material, whereas the FPA pixels are spaced 2 μm apart and contain 20.7 % of exposed epi-grown material.

The change in pixel spacing and amount of exposed epi-grown material had several effects. The first is the etch rate, which were found to be 14-20 % lower for FPA pixels due to the reduced efficiency in both reaction removal and reactant supply. The second was with sidewall morphology. The FPA pixels were found to have more re-deposition on the sidewalls. The re-deposition not only led to more right sidewalls, but also had an impact on the dark current of the devices. In extreme cases, the build is significant such that the sidewalls of the FPA are coated with indium droplets and the arrays appear black. To alleviate this issue, a higher amount of physical etching was incorporated by increasing eh byproduct removal rate relative to the reaction rates. Finally, the last difference is with the sidewall angle. For the FPA pixels, the sidewall angle became more sloped, most likely due to a higher probability of non-directional impinging on the sidewalls. The larger spacing with the test detectors with the test detectors allows for species to undergo fewer collisions and as a result, a 14-20 % differences in sidewall angle.

To transition from dry etching test detectors to dry etching FPA, the optimized etch parameters for the test detectors are initially used as the starting point. Depending on the pixel spacing and amount of exposed epi-grown material, adjustments are made to increase the amount of physical sputtering. This can be done by increasing the bias (10-25 V), adjusting the temperature (± 40-60 ° C), and/or increasing the pressure (5-10 mTorr). Note that changing any of these parameters may negatively affect another characteristic of the etching, so the choice of which parameter to optimize should be made with taking all factors into account. For samples that were primarily dominated by physical sputtering, there was less of a difference in etch rate and a larger change in sidewall angle. As a result, the optimal etch parameters for the test detectors and FPA pixel had less of a disparity. Example cross-sectional SMEs comparing the same etching for test detectors and FPA pixels is shown in Figure 3.

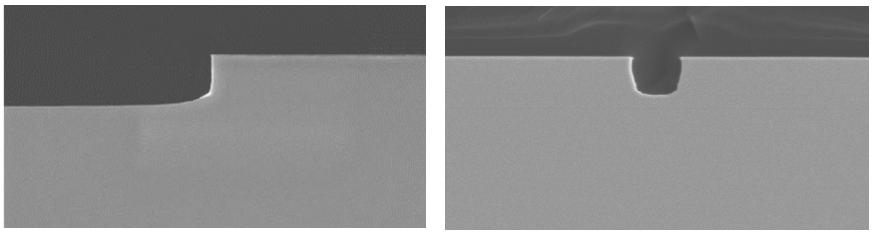

Figure 3. Cross-sectional SEM images of the same etch process used on the same CBIRD material patterned into (left) large 200 μm test detectors spaced 100 μm apart and (right) small 28 μm FPA pixels spaced 2 μm apart. SEM images were captured at a magnification of 15,000x

4. 320 x 256 complementary barrier infrared detector focal plane array

We apply the etching process described above to a 320 x 256 CBIRD LWIR FPA. The FPA is operated at 80 K and image is shown in Figure 4. The etching process achieved a fill factor of 81 % and good uniformity with 97 % operability. The array was operated at a bias of 128 mV, and the measurements yielded a mean dark current of 2.2×10^{-4} A/cm^2 and and NEΔT of 18.6 mK. Using 300 K background illumination and f/2 optics, a mean detectivity of D* = 1.3×10^{11} cm-Hz$^{1/2}$/W was achieved. Full characterization and detailed description of the FPA performance is described in another report [11].

Figure 4. Image taken from a 320 x 256 CBIRD LWIR FPA at T = 80K. The FPA pixels were fully reticulated using the dry etch process described in this work.

Conclusion

We demonstrated improved etching by considering factors that affect the etching process and quality of the SL FPAs. We provided our technique used to properly condition the ICP chamber and clean it to prevent any byproduct re-deposition. We discussed ways to improve the dielectric hard mask quality to reduce interactions from the eroded mask material, straight pattern transfer, and prevent limitations in achieving vertical sidewalls. We further discussed how to achieve good etch uniformity with a practical mounting technique. Finally we dicuss the changes experienced when transitioning from large, sparsely populated test detectors used in the development stage to small, densely packed FPAs. Techniques to account for these changes, how to overcome the challenges, and the optimization process for this have been provided. Finally, the etching process is applied to 320 x 256 CBIRD LWIR FPA work.

Acknowledgement

The authors would like to tank Dr. Meimei Tidrow, Dr. Sumith Bandara, and Dr. Lucy Zheng for encouragement, support, and valuable discussions. The research described in this article was carried out at Jet Propulsion Laboratory, California Institute of Technology, under a contract with National Aeronautics and Space Administration. Copy right 2012 California Institute of Technology. Government sponsorship acknowledged.

Reference

[1] Jean Nguyen, Alexander Soibel, David Z.-Y. Ting, Cory J. Hill, Mike C. Lee, and Sarath D. Gunapala, "Low dark current long-wave infrared InAs/GaSb superlattice detectors", *Appl. Phys. Lett.* **97**, 051108, (2010).

[2] Siew Li Tan, Yu Ling Goh, Sankha dip Das, Shiyong Zhang, Chee Hing Tan, John P. R. David, Nutan Gautam, Hasul Kim, Elena Plis, and Sanjay Krishna, "Dry etching and surface passivation techniques for type-II InAs/GaSb superlattice infrared detectors", *Proc. SPIE* **7838**, 783814-1, (2010).

[3] Edward Kwei-wei Huang, Darin Hoffman, Binh-Minh Nguyen, Pierre-Yves Delaunay, and Manijeh Razeghi, "Surface leakage reduction in narrow band gap type-II antimonide-based superlattice photodiodes", *Appl. Phys. Lett.* **94**, 053506, (2009).

[4] David Z.-Y. Ting, Cory J. Hill, Alexander Soibel, Sam A. Keo, Jason M. Mumolo, Jean Nguyen, and Sarath D. Gunapala, "A high-performance long wavelength superlattice complementary barrier infrared detector", *Appl. Phys. Lett.* **95**, 023508, (2009)

[5] J. W. McNabb, H. G. Craighead, H. Temkin, and R. A. Logan, "Anisotropic reactive ion etching of InP in methane/hydrogen based plasmas", *J. Vac. Sci. Technol. B* **9** (6), 3535, (1991).

[6] James Werking, Jeff Schramm, Chanh Nguyen, Evelyn L. Hu, and Herbert Kroemer, "Methane/hydrogen-based reactive ion etching of InAs, InP, GaAs, and GaSb", *Appl. Phys. Lett.* **58**, 2003, (1991).

[7] Andrew Hood, Pierre-Yves Delaunay, Darin Hoffman, Binh-Minh Nguyen, Yajun Wei, and Manijeh Razeghi, "Near bulk-limited R_0A of long-wavelength infrared type-II InAs/GaSb superlattice photodiodes with polymide surface passivation"*, Appl. Phys. Lett.* **90**, 233513, (2007).

[8] Yiqiao Chen, Aaron Moy, Shangheng Xin, Kan Mi, and Peter P. Chow, "Improvement of R_0A product of type-II InAs/GaSb superlattice MWIR/LWIR photodiodes", *Infrared Phys. Technol.* **52**(6), 340-343, (2009).

[9] B.-T. Lee, T. R. Hayes, P. M. Thomas, R. Pawelek, and P. F. Sciortino Jr., "SiO_2 mask erosion and sidewall composition during CH_4/H_2 reactive ion etching of InGaAsP/InP", *Appl. Phys. Lett.* **63,** 3170, (1993).

[10] A. Baca and C. Ashby, *Fabrication of GaAs Devices*, The Institution of Engineering and Technology, London, 2005.

[11] Sir B. Rafol, A. Soibel, A. Khoshakhlagh, J. Nguyen, J. K. Liu, J. M. Mumolo, S. A. Keo, L. Hoeglund, D. Z. Ting, and S. D. Gunapala, "Performance of a ¼ VGA Format Long-Wavelength Infrared Antimonide Based Superlattice Focal Plane Array", *to be published in IEEE J. Quant. Electron.,* (2012).